

# AC6901A 芯片规格书

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## AC6901A Features

### High performance 32-bit RISC CPU

- RISC 32bit CPU
- DC-160MHz operation
- Support DSP instructions
- 64Vectored interrupts
- 4 Levels interrupt priority

### Flexible I/O

- 30 GPIO pins
- All GPIO pins can be programmable as input or output individually
- All GPIO pins are internal pull-up/pull-down selectable individually
- CMOS/TTL level Schmitt triggered input
- External wake up/interrupt on all GPIOs

### Peripheral Feature

- One full speed USB 2.0 OTG controller
- One audio interface supports IIS, left adjusted, right adjusted and DTP mode
- Four multi-function 16-bit timers, support capture and PWM mode
- Two 16-bit PWM generator for motor driving
- One 16-bit active parallel port
- One full-duplex basic UART
- Two full-duplex advanced UART
- Two SPI interface supports host and device mode
- Two SD Card Host controller
- One IIC interface supports host and device mode
- Watchdog
- 2 Crystal Oscillator
- 16-bit Stereo DAC, SNR > 92dB
- 3 channels Stereo ADC, SNR > 92dB
- 1 channel MIC amplifier
- Embedded headphone amplifier
- 3 channels Stereo analog MUX
- channels 10-bit ADC
- 2 channels 4 levels Low Voltage Detector
- Built in Cap Sense Key controller
- Power-on reset
- Embedded PMU

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### Bluetooth Feature

- CMOS single-chip fully-integrated radio and baseband
- Compliant with Bluetooth V4.2+BR+EDR+BLE specification
- Bluetooth Piconet and Scatternet support
- Meet class2 and class3 transmitting power requirement
- Provides +2dbm transmitting power
- receiver with -85dBm sensitivity
- Support a2dp\avctp\avdtp\avrcp\hfp\spp\smp\att\gap\gatt\rfcomm\sdp\l2cap profile

### FM Tuner

- Support worldwide frequency band 76-108MHz
- Fully integrated digital low-IF tuner & frequency synthesizer
- Autonomous search tuning
- Digital auto gain control (AGC)
- Digital adaptive noise cancellation
- Programmable de-emphasis (50/75 uS)
- Receive signal strength indicator (RSSI)
- Digital volume control

### Power Supply

- LDOIN is 3.3V to 5.5V
- VDDIO is 3.0V to 3.6V

### Packages

- LQFP48

### Temperature

- Operating temperature: -40°C to +85°C
- Storage temperature: -65°C to +150°C

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## 一、引脚定义

### 1.1 引脚分配

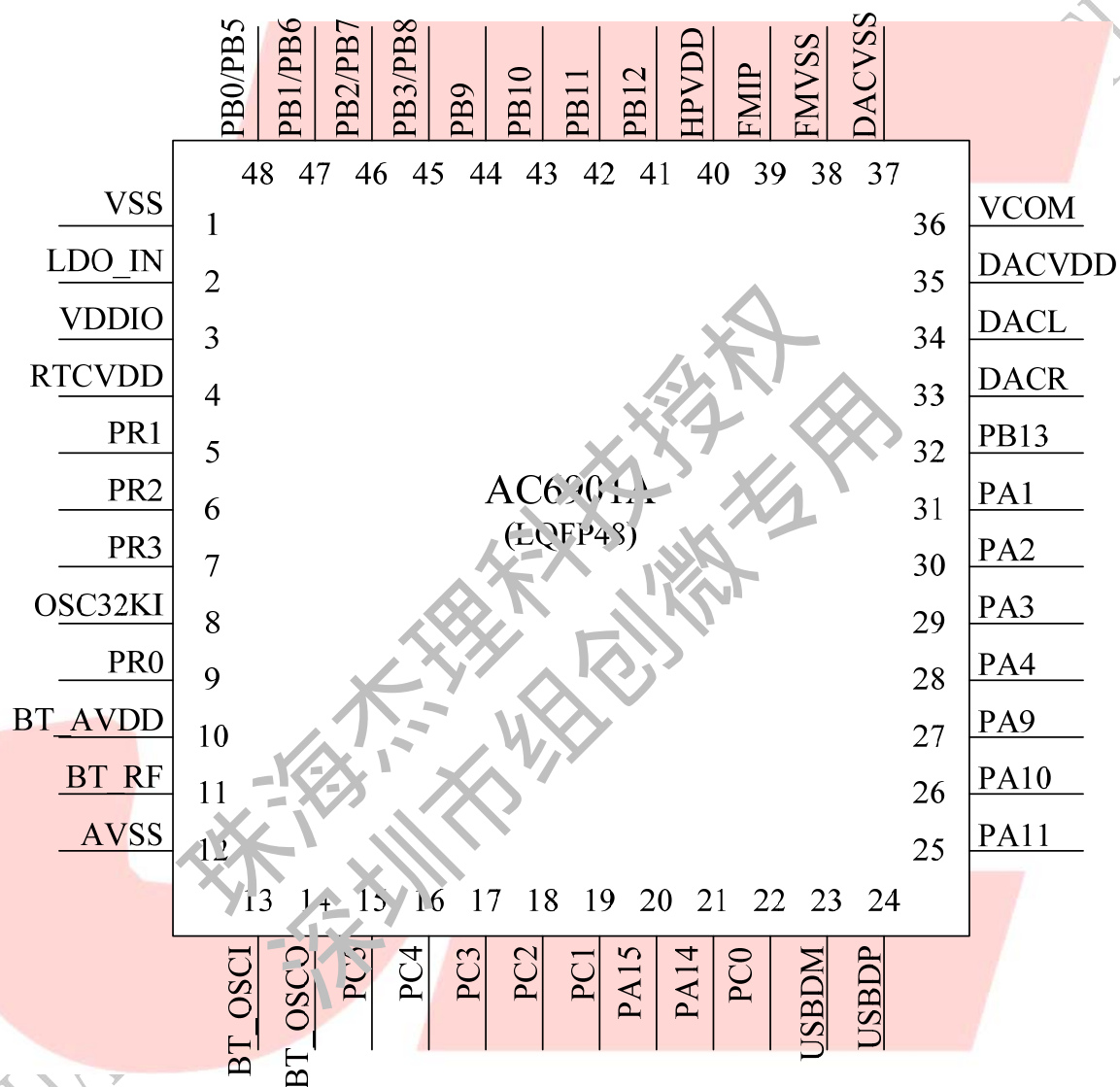


图 1-1 AC6901A\_LQFP48 引脚分配图

## 1.2 引脚描述

表 1-1 AC6901A\_LQFP48 引脚描述

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
1	VSS	P	/	Ground	
2	LDO_IN	P	/	LDO Power	
3	VDDIO	P	/	IO Power 3.3v	
4	RTCVDD	P	/	RTC Power 3.3v	
5	PR1	I/O	16	RTCIO1	ADC12: ADC Input Channel 12;
6	PR2	I/O	16	RTCIO2	ADC13: ADC Input Channel 13;
7	PR3	I/O	16	RTCIO3	OSC1M0
8	OSC32KI	I	/	OSC32KI	
9	PR0	I/O	16	RTCIO0	OSC32K0
10	BT_AVDD	P	/	Power 1.5v	
11	BT_RF	P	/		
12	AVSS	P	/	Ground	
13	BT_OSCI	I	/	OSC In	
14	BT_OSCO	O	/	OSC Out	
15	PC5	I/O	16	GPIO	COM0: LCD COM Output 0; SEG21: LCD SEG Output21; SD1CLKA: SD1 Clk(A); PAPWR: PAP Write; SPI1DOB: SPI1 Data Out(B); UART2RXD: Uart2 Data In(D) IIC_SDA_B: IIC SDA(B);
16	PC4	I/O	16	GPIO	COM1: LCD COM Output 1; SEG20: LCD SEG Output20; SD1CMDA: SD1 Command(A); PAPRD: PAP Read; SPI1CLKB: SPI1 Clk(B); UART2TXD: Uart2 Data Out(D); IIC_SCL_B: IIC SCL(B);
17	PC3	I/O	16	GPIO	COM2: LCD COM Output 2; SEG19: LCD SEG Output19; SD1DAT0A: SD1 Data0(A); PAPD7: PAP Data 7; SPI1DIB: SPI1 Data In(B); UART0RXC: Uart0 Data In(C)

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18	PC2	I/O	16	GPIO	COM3: LCD COM Output 3; SEG18: LCD SEG Output18; SD1DAT1A: SD1 Data1(A); PAPD6: PAP Data 6; SPI2DIB: SPI2 Data In(B); UART0TXC: Uart0 Data Out(C); CAP1: Timer1 Capture;
19	PC1	I/O	16	GPIO	COM4: LCD COM Output 4; SEG17: LCD SEG Output17; SD1DAT2A: SD1 Data2(A); PAPD5: PAP Data 5; SPI2DOB: SPI2 Data Out(B); UART1RXB: Uart1 Data In(B);
20	PA15	I/O	16	GPIO	SEG15: LCD SEG Output15; CAP2: Timer2 Capture; UART0RXD: Uart0 Data In(D) LNA_EN: ALNK_MCLKA: Audio Link Master Clk(A); IIC_SDA_B: IIC SDA(B);
21	PA14	I/O	16	GPIO	SEG14: LCD SEG Output14; TMR1: Timer1 Clock Input; UART0TXD: Uart0 Data Out(D); PA_EN: ALNK_DAT3A: Audio Link Data3(A); IIC_SCL_C: IIC SCL(C); Wakeup4: Port Interrupt /Wakeup 4;
22	PC0	I/O	16	GPIO	COM5: LCD COM Output 5; SEG16: LCD SEG Output16; SD1DAT3A: SD1 Data3(A); PAPD4: PAP Data 4; SPI2CLKB: SPI2 Clk(B); UART1TXB: Uart1 Data Out(B);
23	USBDM	I/O	4	USB Negative Data	ISP_DI:
24	USBDP	I/O	4	USB Positive Data	ISP_DO:
25	PA11	I/O	16	GPIO	SEG11: LCD SEG Output11; SD0DAT0A: SD0 Data0(A); ALNK_DAT0A: Audio Link Data0(A);
26	PA10	I/O	16	GPIO	SEG10: LCD SEG Output10; SD0DAT1A: SD0 Data1(A); UART2RXB: Uart2 Data In(B);

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					ADC5: ADC Input Channel 5; ALNK_LRCKA: Audio Link Clk(A); PAPD3: PAP Data3; Wakeup3: Port Interrupt /Wakeup 3;
27	PA9	I/O	16	GPIO	SEG9: LCD SEG Output9; SD0DAT2A: SD0 Data2(A); UART2TXB: Uart2 Data Out(B); ADC4: ADC Input Channel 4; ALNK_SCLKA: Audio Link Clk(A); PAPD2: PAP Data2;
28	PA4	I/O	16	GPIO	SEG4: LCD SEG Output4; AMUX1R: Simulator Channel1 Right; Touch11: Touch Input Channel 11; ADC1: ADC Input Channel 1; UART2RXA: Uart2 Data In(A); PWM1: Timer1 PWM Output;
29	PA3	I/O	16	GPIO	SEG3: LCD SEG Output3; AMUX1L: Simulator Channel 1 Left; Touch10: Touch Input Channel 10; ADC0: ADC Input Channel 0; UART2TXA: Uart2 Data Out(A); ISP_CLK; Wakeup8: Port Interrupt /Wakeup 8;
30	PA2	I/O	16	GPIO	SEG2: LCD SEG Output2; AMUX0R: Simulator Channel0 Right; Touch9: Touch Input Channel 9; CAP3: Timer3 Capture; UART1RXC: Uart1 Data In(C);
31	PA1	I/O	16	GPIO	SEG1: LCD SEG Output1; AMUX0L: Simulator Channel0 left; Touch8: Touch Input Channel 8; PWM0: Timer0 PWM Output; UART1TXC: Uart1 Data Out(C);
32	PB13	I/O	16	GPIO	MIC
33	DACR	O	/	DAC Right Channel	

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34	DACL	O	/	DAC Left Channel	
35	DACVDD	P	/	DAC Power	
36	VCOM	P	/	DAC Reference	
37	DACVSS	P	/	DAC Ground	
38	FMVSS	P	/		
39	FMIP	I	/		
40	HPVDD	P	/		
41	PB12	I/O	24	GPIO	AMUX2R: Simulator Channel2 Right; NFCRX: NFC Data In Touch7: Touch Input Channel 7; ADC11: ADC Input Channel 11; SPI1DOA: SPI1 Data Out(A); SFC_CLKB:SD0 Clk(B);
42	PB11	I/O	24	GPIO	AMUX2L: Simulator Channel2 Left; NFCTX: NFC Data Out Touch6: Touch Input Channel 6; ADC10: ADC Input Channel 10; SPI1CLKA: SPI1 Clk(A); SD0CMDDB: SD0 Command(B); Wakeup13: Port Interrupt /Wakeup 13;
43	PB10	I/O	24	GPIO	UART2RXC: Uart2 Data In(C); Touch5: Touch Input Channel 5; ADC9: ADC Input Channel 9; SPI1_DIA: SPI1 Data In(A); SD0DAT0B: SD0 Data0(B); CAP0: Timer0 Capture;
44	PB9	I/O	24	GPIO	UART2TXC: Uart2 Data Out(C); ADC8: ADC Input Channel 8; CLKOUT1: Clk Out1; SD0DAT1B: SD0 Data1(B); Wakeup12: Port Interrupt /Wakeup 12;
45	PB8	I/O	24	GPIO	SFC_CLKB: SFC Clock(B); SPI0_CLKB: SPI0 Clock(B); ADC7: ADC Input Channel 7; SD0DAT2B: SD0 Data2(B);
	PB3	I/O	24	GPIO	PWM2: Timer2 PWM Output; SPI0_DAT3AB: SPI0 Data 3(AB); SFC_DAT3AB: SFC Data 2(AB);

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					SD1DAT1B: SD1 Data1(B); ALNK_DAT1B : Audio Link Data1(B); Touch3: Touch Input Channel 3;
46	PB7	I/O	24	GPIO	SFC_DOB(0): SFC Data Out0(B); SPI0_DOB(0): SPI0 Data Out0(B); UART0RXB: Uart0 Data In(B); ADC6: ADC Input Channel 6; TMR3: Timer3 Clock Input; SD0DAT3B: SD0 Data3(B);
	PB2	I/O	24	GPIO	SPI2DIA: SPI2 Data In(A); SD1CLKB: SD1 Clk(B); ALNK_DAT0B: Audio Link Data0(B); Touch2: Touch Input Channel 2; Wakeup11: Port Interrupt /Wakeup 11;
47	PB6	I/O	24	GPIO	SFC_CSB: SFC Chip Select(B); SPI0_CSB: SPI0 Chip Select(B); UART0TXB: Uart0 Data Out(B); ALNK_MCLKB: Audio Link Master Clk(B);
	PB1	I/O	24	GPIO	TMR2: Timer2 Clock Input; UART1RXA: Uart1 Data In(A); SPI2DOA: SPI2 Data Out(A); SD1CMDB: SD1 Command(B); ALNK_LRCKB : Audio Link Clk(B); Touch1: Touch Input Channel 1;
	PB5	I/O	24	GPIO	SFC_DIB(1): SFC Data In1(B); SPI0_DIB(1): SPI0 Data In1(B); SD1DAT3B: SD1 Data3(B); ALNK_DAT3B: Audio Link Data3(B);
48	PB0	I/O	24	GPIO	CLKOUT1: Clk Out1; UART1TXA: Uart1 Data Out(A); SPI2CLKA: SPI2 Clk(A); SD1DAT0B: SD1 Data0(B); ALNK_SCLKB: Audio Link Clk(B); Touch0: Touch Input Channel 0; Wakeup10: Port Interrupt /Wakeup 10;

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## 二、电气特性

### 2.1 PMU 电压、电流特性

表 2-1

符号	参数	最小	典型	最大	单位	测试条件
LDOIN	Voltage Input	3	3.7	5.5	V	
$V_{3.3}$	Voltage output	-	3.3	-	V	LDO5V = 5V, 100mA loading
$V_{1.2}$		-	1.2	-	V	LDO5V = 5V, 50mA loading
$V_{1.5}$	Voltage output		1.5		V	LDO5V=5V, 100mA loading
$V_{DACVDD}$	DAC Voltage	-	3.1	-	V	LDO5V = 5V, 10mA loading
$I_{L3.3}$	Loading current	-	-	150	mA	LDO5V = 5V

### 2.2 IO 输入、输出高低逻辑特性

表 2-2

IO 输入特性						
符号	参数	最小	典型	最大	单位	测试条件
$V_{IL}$	Low-Level Input Voltage	-0.2	-	$0.3 \times V_{DDIO}$	V	$V_{DDIO} = 3.3V$
$V_{IH}$	High-Level Input Voltage	$0.7 \times V_{DDIO}$	-	$V_{DDIO} + 0.3$	V	$V_{DDIO} = 3.3V$
IO 输出特性						
$V_{OL}$	Low-Level Output Voltage	-	-	0.33	V	$V_{DDIO} = 3.3V$
$V_{OH}$	High-Level Output Voltage	2.7	-	-	V	$V_{DDIO} = 3.3V$

### 2.3 IO 输出能力、上下拉电阻特性

表 2-3

Port 口	普通输出	强输出	上拉电阻	下拉电阻	备注
PA0~PA15 PB13 PC0~PC5 PR0~PR3	串接 200 欧电阻（寄存器可控制）	16mA	10K	60K	1、PA3 default pulldown 2、PB6 default pullup 3、PR0 output 0 4、内部上下拉阻抗因工艺波动差异，可能存在±20%的偏差
PB0~PB12	8mA	24mA	10K	60K	
USBDM USBDP	4mA	-	1.5K	15K	

## 2.4 DAC 特性

参数	最小	典型	最大	单位	测试条件
Frequency Response	20	-	200000	Hz	1KHz/0dB 10Kohm loading With A-Weighted Filter
THD+N	-	-71	-	dB	
S/N	-	93	-	dB	
Crosstalk	-	-90	-	dB	
Output Swing	-	1.08	-	Vrms	
Dynamic Range	-	93	-	dB	1KHz/-60dB 10Kohm loading With A-Weighted Filter
DAC Output Power	-	>11	-	mW	32ohm loading

## 2.5 ADC 特性

参数	最小	典型	最大	单位	测试条件
Dynamic Range	-	93	-	dB	1KHz/-60dB 10Kohm loading With A-Weighted Filter
S/N	-	92	-	dB	1KHz/-60dB
THD+N	-	-75	-	dB	10Kohm loading
Crosstalk	-	-80	-	dB	With A-Weighted Filter

## 2.6 BT 特性

表 2-4

参数	最小	典型	最大	单位	测试条件
Maximum Output Power	-	2	-	dBm	-
RMS DEVM	-	5.3	-	%	Maximum output power
PEAK DEVM	-	12	-	%	
99% DEVM	-	8	-	%	
EDR Relative Power	-	-1.4	-	dB	
BDR Sensitivity	-	-84	-	dBm	BER=0.001
EDR Sensitivity	-	-86	-	dBm	BER=0.0001

### 三、封装

#### 3.1 LQFP48\_7\*7

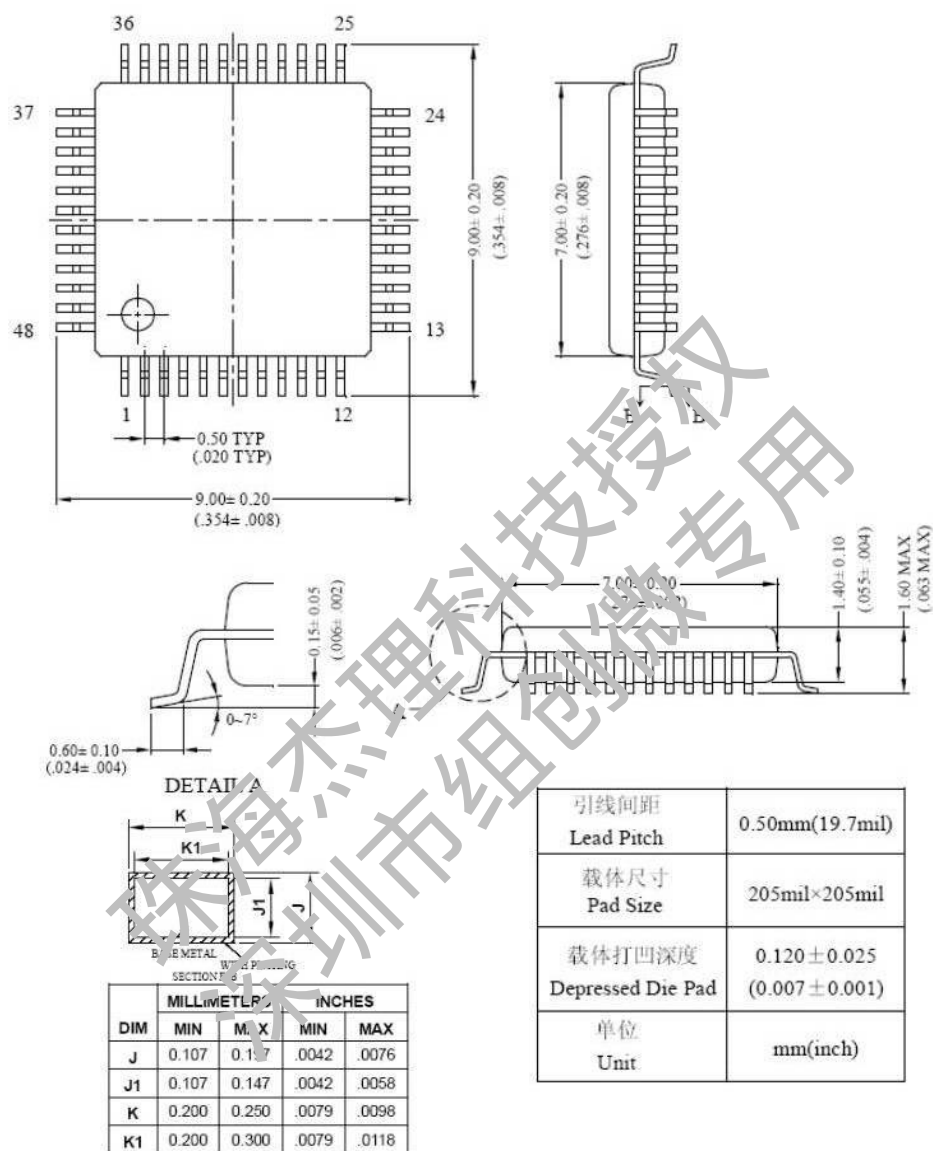


图 3-1 AC6901A\_LQFP48 封装图

#### 四、版本信息

日期	版本号	描述
2016.09.12	V1.0	原始版本
2016.12.14	V1.1	升级蓝牙版本为 4.2，增加可支持的蓝牙协议
2016.12.22	V1.2	规范统一蓝牙 4.2 版本格式

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